UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/787,166	02/27/2004	Minoru Okamoto	61282-064	4892

7590 06/05/2006

McDERMOTT, WILL & EMERY
600 13th Street, N.W.
Washington, DC 20005-3096

EXAMINER	
LAM, NELSON C	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 06/05/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/787,166	OKAMOTO, MINORU	
	Examiner	Art Unit	
	Nelson Lam	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *05/27/2004*. 4/25/06
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Responsive to communication on 02/27/2004. Application 10/787,166 has been examined. In the examination of 10/787,166, claims 1-29 are pending.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. **Claims 1, 3, 5, 7, 9, 11, 13-14, 16, 18, 20, 22, 24 and 26-29 are rejected under 35 U.S.C. 102(b)** as being anticipated by Yonezawa et al. (US Patent No. 6,513,146).

As per **claim 1**, Yonezawa discloses System LSI design support apparatus which supports a design for assigning system features to a system LSI comprising processing units having a plurality of different architectures, said apparatus having as an input a program describing system features in a high-level language, comprising:

a function extractor, which extracts functions described in the program (Yonezawa: Fig. 1, #ST11; Figs. 4(a), 4(b); col. 1, line 52-67; col. 8, line 31-46; col. 9, line 13-35);

an analyzer, which counts the number of conditional branch statements described in each function extracted by the function extractor (Yonezawa: col. 3, line 60 to col. 4, line 11; col. 4, line 14-27; col. 9, line 13-35; col. 9, line 36-57; Fig. 1, #ST13, #ST16; col. 10, line 17-25); and

a calculation section, which outputs calculation result information based on the counting results of the analyzer for each function extracted by the function extractor (Yonezawa: Fig. 3; col. 9, line 35-57; col. 9, line 64 to col. 10, line 16).

As per **claim 3**, Yonezawa discloses the system LSI design support apparatus according to claim 1, wherein, based on the calculation process of variables related to the conditions of the conditional branch statements described in each function extracted by the function extractor, the analyzer counts the number of functions required to generate the variables (Yonezawa: col. 3, line 60 to col. 4, line 11; col. 4, line 14-27; col. 9, line 13-35; col. 9, line 36-57; Fig. 1, #ST13, #ST16; col. 10, line 17-25).

As per **claim 5**, Yonezawa discloses system LSI design support apparatus which supports a design for assigning system features to a system LSI comprising processing units having a plurality of different architectures, said apparatus having as an input a program describing system features in a high-level language, comprising:

a function extractor, which extracts functions described in the program (Yonezawa: Fig. 1, #ST11; Figs. 4(a), 4(b); col. 1, line 52-67; col. 8, line 31-46; col. 9, line 13-35);

an analyzer, which counts the number of loop control statements described in each function extracted by the function extractor (Yonezawa: col. 3, line 60 to col. 4, line 11; col. 4, line 14-27; col. 9, line 13-35; col. 9, line 36-57; Fig. 1, #ST13, #ST16; col. 10, line 17-25); and

a calculation section, which outputs calculation result information based on the counting results of the analyzer for each function extracted by the function extractor (Yonezawa: Fig. 3; col. 9, line 35-57; col. 9, line 64 to col. 10, line 16).

As per **claim 7**, Yonezawa discloses the system LSI design support apparatus according to claim 5, wherein, based on the calculation process of variables related to the number of repetitions of loop control statements described in each function extracted by the function extractor, the analyzer counts the number of functions required to generate the variables (Yonezawa: col. 3, line 60 to col. 4, line 11; col. 4, line 14-27; col. 9, line 13-35; col. 9, line 36-57; Fig. 1, #ST13, #ST16; col. 10, line 17-25).

As per **claim 9**, Yonezawa discloses system LSI design support apparatus which supports a design for assigning system features to a system LSI comprising processing units having a plurality of different architectures, said apparatus having as an input a program describing system features in a high-level language, comprising:

a function extractor, which extracts functions described in the program (Yonezawa: Fig. 1, #ST11; Figs. 4(a), 4(b); col. 1, line 52-67; col. 8, line 31-46; col. 9, line 13-35);

an analyzer, which counts the number of conditional branch statements and loop control statements described in each function extracted by the function extractor (Yonezawa: col. 3, line 60 to col. 4, line 11; col. 4, line 14-27; col. 9, line 13-35; col. 9, line 36-57; Fig. 1, #ST13, #ST16; col. 10, line 17-25); and

a calculation section, which outputs calculation result information where the counting results of the analyzer are summed for each function extracted by the function extractor (Yonezawa: Fig. 3; col. 9, line 35-57; col. 9, line 64 to col. 10, line 16).

As per **claim 11**, Yonezawa discloses the system LSI design support apparatus according to claim 9, wherein, based on the calculation process of variables related to the number of repetitions of the conditional branch statements and loop control statements described in each function extracted by the function extractor, the analyzer counts the number of functions required to generate the variables (Yonezawa: col. 3, line 60 to col. 4, line 11; col. 4, line 14-27; col. 9, line 13-35; col. 9, line 36-57; Fig. 1, #ST13, #ST16; col. 10, line 17-25).

As per **claim 13**, Yonezawa discloses the system LSI design support apparatus according to claim 1, wherein the function extractor comprises:

function combination means, which specifies at least one of the plurality of sets of functions arbitrarily selected from the functions extracted by the function extractor and that the analyzer performs analysis of each set of functions specified by the function combination means. (Yonezawa: Fig. 1, #ST11; Figs. 4(a), 4(b); col. 1, line 52-67; col. 8, line 31-46; col. 9, line 13-35).

As per **claim 14**, Yonezawa discloses a system LSI design support method which supports a design for assigning system features to a system LSI comprising processing units having a plurality of different architectures, comprising steps of:

inputting a program describing system features in a high-level language (Yonezawa: col. 27, line 57 to col. 28, line 4; col. 28, line 13-23);

extracting functions described in the program (Yonezawa: Fig. 1, #ST11; Figs. 4(a), 4(b); col. 1, line 52-67; col. 8, line 31-46; col. 9, line 13-35);

counting the number of conditional branch statements described in each function extracted (Yonezawa: col. 3, line 60 to col. 4, line 11; col. 4, line 14-27; col. 9, line 13-35; col. 9, line 36-57; Fig. 1, #ST13, #ST16; col. 10, line 17-25); and

outputting calculation result information based on the counting results for each function extracted (Yonezawa: Fig. 3; col. 9, line 35-57; col. 9, line 64 to col. 10, line 16).

As per **claim 16**, Yonezawa discloses the system LSI design support method according to claim 14, further comprising the steps of:

counting, based on the calculation process of variables related to the conditions of the conditional branch statements described in the each function extracted, the number of functions required to generate the variables (Yonezawa: col. 3, line 60 to col. 4, line 11; col. 4, line 14-27; col. 9, line 13-35; col. 9, line 36-57; Fig. 1, #ST13, #ST16; col. 10, line 17-25).

As per **claim 18**, Yonezawa discloses a system LSI design support method which supports a design for assigning system features to a system LSI comprising processing units having a plurality of different architectures, comprising steps of:

inputting a program describing system features in a high-level language (Yonezawa: col. 27, line 57 to col. 28, line 4; col. 28, line 13-23);

extracting functions described in the program (Yonezawa: Fig. 1, #ST11; Figs. 4(a), 4(b); col. 1, line 52-67; col. 8, line 31-46; col. 9, line 13-35);

counting the number of loop control statements described in each function extracted (Yonezawa: col. 3, line 60 to col. 4, line 11; col. 4, line 14-27; col. 9, line 13-35; col. 9, line 36-57; Fig. 1, #ST13, #ST16; col. 10, line 17-25); and

outputting calculation result information based on the counting results are summed for each function extracted (Yonezawa: Fig. 3; col. 9, line 35-57; col. 9, line 64 to col. 10, line 16).

As per **claim 20**, Yonezawa discloses the system LSI design support method according to claim 18, further comprising the steps of:

counting, based on the calculation process of variables related to the number of repetitions of the loop control statements described in the each function extracted, the number of functions required to generate the variables (Yonezawa: col. 3, line 60 to col. 4, line 11; col. 4, line 14-27; col. 9, line 13-35; col. 9, line 36-57; Fig. 1, #ST13, #ST16; col. 10, line 17-25);

As per **claim 22**, Yonezawa discloses a system LSI design support method which supports a design for assigning system features to a system LSI comprising processing units having a plurality of different architectures, comprising steps of:

inputting a program describing system features in a high-level language (Yonezawa: col. 27, line 57 to col. 28, line 4; col. 28, line 13-23);

extracting functions described in the program (Yonezawa: Fig. 1, #ST11; Figs. 4(a), 4(b); col. 1, line 52-67; col. 8, line 31-46; col. 9, line 13-35);

counting the number of conditional branch statements and loop control statements described in each function extracted (Yonezawa: col. 3, line 60 to col. 4, line

11; col. 4, line 14-27; col. 9, line 13-35; col. 9, line 36-57; Fig. 1, #ST13, #ST16; col. 10, line 17-25); and

outputting calculation result information where the counting results for each function extracted (Yonezawa: Fig. 3; col. 9, line 35-57; col. 9, line 64 to col. 10, line 16).

As per **claim 24**, Yonezawa discloses the system LSI design support method according to claim 22 , further comprising the steps of:

counting, based on the calculation process of variables related to the conditions of the conditional branch statements and those related to the number of repetitions of the loop control statements described in the each function extracted, the number of functions required to generate said variables (Yonezawa: col. 3, line 60 to col. 4, line 11; col. 4, line 14-27; col. 9, line 13-35; col. 9, line 36-57; Fig. 1, #ST13, #ST16; col. 10, line 17-25).

As per **claim 26**, Yonezawa discloses the system LSI design support method according to claim 14, further comprising the steps of:

specifying at least one of the plurality of sets of functions arbitrarily selected from the functions extracted, wherein the specifying performs the calculation of each of the specified sets of functions (Yonezawa: Fig. 1, #ST11; Figs. 4(a), 4(b); col. 1, line 52-67; col. 8, line 31-46; col. 9, line 13-35).

As per **claim 27**, Yonezawa discloses database apparatus (Yonezawa: Fig. 7(b), #10; Fig. 8(b), #10; col. 16, line 46-56) for storing data to be provided to system LSI design support apparatus which supports a design for assigning system features to a

system LSI comprising processing units having a plurality of different architectures, wherein the data concerns to a program describing system features in a high-level language and the data is definition information where a number of conditional branch statements processed by the processing unit is defined per separate processing unit (Yonezawa: col. 3, line 60 to col. 4, line 11; col. 4, line 14-27; col. 9, line 13-35; col. 9, line 36-57; Fig. 1, #ST13, #ST16; col. 10, line 17-25).

As per **claim 28**, Yonezawa discloses database apparatus (Yonezawa: Fig. 7(b), #10; Fig. 8(b), #10; col. 16, line 46-56) for storing data to be provided to system LSI design support apparatus which supports a design for assigning system features to a system LSI comprising processing units having a plurality of different architectures, wherein the data concerns to a program describing system features in a high-level language and the data is definition information where a number of loop control statements processed by the processing unit is defined per separate processing unit (Yonezawa: col. 3, line 60 to col. 4, line 11; col. 4, line 14-27; col. 9, line 13-35; col. 9, line 36-57; Fig. 1, #ST13, #ST16; col. 10, line 17-25).

As per **claim 29**, Yonezawa discloses database apparatus (Yonezawa: Fig. 7(b), #10; Fig. 8(b), #10; col. 16, line 46-56) for storing data to be provided to system LSI design support apparatus which supports a design for assigning system features to a system LSI comprising processing units having a plurality of different architectures, wherein the data concerns to a program describing system features in a high-level language and that said data is definition information where a number of conditional branch statements and loop control statements processed by the processing unit is

defined per separate processing unit (Yonezawa: col. 3, line 60 to col. 4, line 11; col. 4, line 14-27; col. 9, line 13-35; col. 9, line 36-57; Fig. 1, #ST13, #ST16; col. 10, line 17-25).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. **Claims 2, 4, 6, 8, 10, 12, 15, 17, 19, 21, 23 and 25 are rejected under 35 U.S.C. 103(a)** as being unpatentable over Yonezawa in view of Gutberlet et al. (US Patent Application Publication No. US 2003/0033039 A1). Yonezawa discloses a method of designing a semiconductor integrated circuit. However, Yonezawa does not disclose the use of nestings of conditional branch statements. Gutberlet discloses a method of designing a semiconductor integrated circuit that includes the use of nestings of conditional branch statements that Yonezawa does not disclose. Therefore, it would be obvious to one of ordinary skill in the art at the time the invention was made to include the use of nestings of conditional branch statements in the method of Gutberlet in the method of Yonezawa because Yonezawa's invention is improved by accurately showing the timing and scheduling of a design (Gutberlet: [0018]; [0029]; [0030]).

As per **claim 2**, Yonezawa in view of Gutberlet discloses the system LSI design support apparatus according to claim 1, wherein the analyzer counts the number of nestings of the conditional branch statements described in each function extracted by

the function extractor (Yonezawa: [0025]; [0027]; [0091]; [0092]; Fig. 1, #ST13, #ST16; [0095]; [0096]) (Gutberlet: Fig. 1; [0005]; [0008]; [0012]; [0013]; [0018]).

As per **claim 4**, Yonezawa in view of Gutberlet discloses the system LSI design support apparatus according to claim 1, further comprising;

mapping means, which compares definition information where a plurality of combinations selected out of the number of conditional branch statements processed by the processing unit, the number of nestings of the conditional branch statements and the number of functions required to generate variables related to the conditions of the conditional branch statements are defined per separate processing unit, with calculation result information output from the calculation section to map an appropriate processing unit to each function (Gutberlet: Fig. 1; [0005]; [0008]; [0012]; [0013]; [0018]).

As per **claim 6**, Yonezawa in view of Gutberlet discloses the system LSI design support apparatus according to claim 5, wherein the analyzer counts the number of nestings of the loop control statements described in each function extracted by the function extractor (Yonezawa: [0025]; [0027]; [0091]; [0092]; Fig. 1, #ST13, #ST16; [0095]; [0096]) (Gutberlet: Fig. 1; [0005]; [0008]; [0012]; [0013]; [0018]).

As per **claim 8**, Yonezawa in view of Gutberlet discloses the system LSI design support apparatus according to claim 5, further comprising:

mapping means, which compare definition information where a plurality of combinations selected out of the number of loop control statements processed by the processing unit, the number of nestings of the loop control statements and the number of functions required to generate variables related to the number of repetitions of the

loop control statements are defined per separate processing unit, with calculation result information output from the calculation section to map an appropriate processing unit to each function (Yonezawa: [0025]; [0027]; [0091]; [0092]; [0094]; [0095]; [0096]) (Gutberlet: Fig. 1; [0005]; [0008]; [0012]; [0013]; [0018]).

As per **claim 10**, Yonezawa in view of Gutberlet discloses the system LSI design support apparatus according to claim 9, wherein the analyzer counts the number of nestings of the conditional branch statements and loop control statements described in each function extracted by the function extractor (Yonezawa: [0025]; [0027]; [0091]; [0092]; Fig. 1, #ST13, #ST16; [0095]; [0096]) (Gutberlet: Fig. 1; [0005]; [0008]; [0012]; [0013]; [0018]).

As per **claim 12**, Yonezawa in view of Gutberlet discloses the system LSI design support apparatus according to claim 9, further comprising:

mapping means, which compares definition information where a plurality of combinations selected out of the number of conditional branch statements and loop control statements processed by the processing unit, the number of nestings of the conditional branch statements and loop control statements, and the number of functions required to generate variables related to the number of repetitions of the conditional branch statements and loop control statements are defined per separate processing unit, with calculation result information output from the calculation section to map an appropriate processing unit to each function (Yonezawa: [0025]; [0027]; [0091]; [0092]; [0094]; [0095]; [0096]) (Gutberlet: Fig. 1; [0005]; [0008]; [0012]; [0013]; [0018]).

As per **claim 15**, Yonezawa in view of Gutberlet discloses the system LSI design support method according to claim 14, further comprising the steps of:

counting the number of nestings of the conditional branch statements described in the each function extracted (Yonezawa: [0025]; [0027]; [0091]; [0092]; Fig. 1, #ST13, #ST16; [0095]; [0096]) (Gutberlet: Fig. 1; [0005]; [0008]; [0012]; [0013]; [0018]).

As per **claim 17**, Yonezawa in view of Gutberlet discloses the system LSI design support method according to claim 14, further comprising the steps of: inputting definition information where a plurality of combinations selected out of the number of conditional branch statements processed by the processing unit, the number of nestings of the conditional branch statements and the number of functions required to generate variables related to the conditions of the conditional branch statements are defined per separate processing unit (Gutberlet: Fig. 1; [0005]; [0008]; [0012]; [0013]; [0018]); and

comparing the definition information with the calculation result information to map an appropriate processing unit to each function (Yonezawa: [0025]; [0027]; [0091]; [0092]; [0094]; [0095]; [0096])

As per **claim 19**, Yonezawa in view of Gutberlet discloses the system LSI design support method according to claim 18, further comprising the steps of:

counting the number of nestings of the loop control statements described in the each function extracted (Yonezawa: [0025]; [0027]; [0091]; [0092]; Fig. 1, #ST13, #ST16; [0095]; [0096]) (Gutberlet: Fig. 1; [0005]; [0008]; [0012]; [0013]; [0018]).

As per **claim 21**, Yonezawa in view of Gutberlet discloses the system LSI design support method according to claim 18, further comprising the steps of:

inputting definition information where a plurality of combinations selected out of the number of loop control statements processed by the processing unit (Yonezawa: [0025]; [0027]; [0091]; [0092]; Fig. 1, #ST13, #ST16; [0095]; [0096]),

the number of nestings of the loop control statements and the number of functions required to generate variables related to the number of repetitions of the loop control statements are defined per separate processing unit; and comparing the definition information with the calculation result information to map an appropriate processing unit to each function (Yonezawa: [0025]; [0027]; [0091]; [0092]; [0094]; [0095]; [0096]) (Gutberlet: Fig. 1; [0005]; [0008]; [0012]; [0013]; [0018]).

As per **claim 23**, Yonezawa in view of Gutberlet discloses the system LSI design support method according to claim 22, further comprising the steps of:

counting the number of nestings of the conditional branch statements and loop control statements described in the each function extracted (Yonezawa: [0025]; [0027]; [0091]; [0092]; Fig. 1, #ST13, #ST16; [0095]; [0096]) (Gutberlet: Fig. 1; [0005]; [0008]; [0012]; [0013]; [0018]).

As per **claim 25**, Yonezawa in view of Gutberlet discloses the system LSI design support method according to claim 22, further comprising the steps of:

inputting definition information where a plurality of combinations selected out of the number of conditional branch statements and loop control statements processed by the processing unit, the number of nestings of the conditional branch statements and loop control statements, and the number of functions required to generate variables related to the conditions of the conditional branch statements and those related to the

number of repetitions of the loop control statements are defined per separate processing unit; and comparing the definition information with the calculation result information to map an appropriate processing unit to each function (Yonezawa: [0025]; [0027]; [0091]; [0092]; [0094]; [0095]; [0096]) (Gutberlet: Fig. 1; [0005]; [0008]; [0012]; [0013]; [0018]).

Conclusion

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nelson Lam whose telephone number is 571 272-8318. The examiner can normally be reached on Monday-Friday from 9am - 5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on 571 272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Nelson Lam
Assistant Examiner
Art Unit 2825

A. M. Thompson
Primary Examiner
Technology Center 2800